

Amendments to the Specification:

Please amend paragraph number [001] as follows:

[001] This is a divisional of U.S. Application Serial No. 09/007,949, filed on January 16, 1998, now U.S. Patent 6,713,384, issued March 30, 2004, which is a divisional of U.S. Application Serial No. 08/811,124, filed on March 3, 1997, now U.S. Patent No. 6,593,657 B1- 6,593,657, issued July 15, 2003.

Please amend paragraph number [002] as follows:

[002] The present invention relates to methods of making a plug and metallization line structure in microelectronic devices. ~~More particularly~~ particularly, the present invention relates to methods of minimizing resistance in the interface between plugs or contacts and the metallization lines connected to them. The present invention is also particularly drawn to methods of minimizing electromigration due to minimized interface resistance and selected alloying. The present invention is also drawn to improving depth-of-focus restrictions in the process of connecting plugs or contacts to metallization lines.

Please amend paragraph number [009] as follows:

[009] Al-Cu electromigration in a structure with Al-Cu metallization lines and Ti or W plugs is well established. The phenomenon occurs because Cu diffusivity through Ti or W is much lower than through Al. ~~Therefore~~ Therefore, the Cu is depleted from the area of the Ti or W plug by the current flow and not replaced, leading to failure at the interface between the Ti or W plug and the Al-Cu metallization lines.

Please amend paragraph number [010] as follows:

[010] Metal creep, on the other hand, occurs due to the differences in the thermal coefficients of expansion between metals, insulators, and silicon wafers. The differences in thermal coefficients of expansion can build up stress in the metallization lines, which can lead to migration of atoms in the metallization line to the various areas of high stress and strain. This migration of atoms forms voids or vacancies in the metallization line ~~which~~ that can cause creep

failure. Additional solutions ~~which~~ that can control both the electromigration and metal creep problems are desirable.

Please amend paragraph number [013] as follows:

[013] The present invention is drawn to methods of making a semiconductor substrate having thereon plug or contact connections to metallization lines, which methods minimize electrical resistance, relieve depth-of-focus restrictions during patterning of the metallization lines, and resist electromigration and creep failure between the plug or contact and the metallization line. In the context of this document, the term “semiconductor substrate” is defined to mean any construction comprising semiconductive material, ~~including~~ including, but not limited ~~to~~ to, bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term “substrate” refers to any supporting structure ~~including~~ including, but not limited ~~to~~ to, the semiconductor substrates described above.

Please amend paragraph number [014] as follows:

[014] A first method of the present invention comprises patterning a contact hole within an insulation layer situated on a semiconductor substrate or equivalent. The contact hole can be for a via, interconnect, or bit line. A first metal layer is then formed upon the insulation layer. If necessary for complete filling of the contact hole, additional steps are carried out by such methods as reflow or pressure fill. The first metal layer is then planarized to isolate a plug of the first metal layer in the contact hole within the insulation layer. After isolating the plug in the contact hole, a second metal layer is formed upon the insulation layer over and on an exposed end of the isolated plug. The second metal layer may then be planarized to a preferred thickness so as to render the same with a photo-notching resistant surface that alleviates stringent ~~depth-of-focus~~ depth-of-focus requirements in forming metallization lines. Finally, metallization lines are patterned out of the second metal layer. The first and second metal layers can be composed of either a substantially pure metal or an alloy thereof.

Please amend paragraph number [015] as follows:

[015] A second method of the present invention comprises patterning a contact hole within an insulation layer situated on a substrate assembly or equivalent. A single layer of metal is then formed upon the insulation layer. If necessary for complete ~~filling~~ filling of the contact hole, additional steps are carried out by such methods as reflow or pressure fill. The single layer of metal is then planarized above the insulation layer to a thickness that is preferred for metallization lines. Finally, the single layer of metal is patterned to create therefrom a unitary structure of both metallization lines and a plug isolated in the contact ~~hole of~~ hole within the insulation layer. The single layer of metal can be composed of either a substantially pure metal or an alloy thereof.

Please amend paragraph number [019] as follows:

[019] In order to illustrate the manner in which the above-recited and other features of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof ~~which~~ that are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are ~~not therefore~~ not, therefore, to be considered limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Please amend paragraph number [020] as follows:

[020] Figure 1 is a cross-sectional view of a planarized insulation layer having therein a contact hole, the insulation layer being situated on a semiconductor substrate, and a metallization layer being disposed upon the insulation layer over the contact hole ~~which~~ that is not filled by the metallization layer.

Please amend paragraph number [028] as follows:

[028] The present invention comprises methods to overcome technical challenges in the prior art and structures achieved thereby. Materials used in the present invention are preferred but are illustrative of non-limiting examples by which the present invention can be carried out with equivalent materials, either by ~~resort~~ resorting to the specification or by practicing the invention as disclosed herein.

Please amend paragraph number [029] as follows:

[029] A preferred material in the methods of the present invention is boron phosphorus silicate glass (BPSG) for an insulation layer in which a contact hole is provided. The insulation layer may also be composed of TEOS, doped silicon dioxide, BPSG, PSG, BSG, and silicon nitride, where TEOS is an oxide of silicon deposited in a chemical vapor deposition (CVD) process using a tetraethylorthosilicate precursor. The insulation layer is preferably situated on a semiconductor substrate of a semiconductor wafer. Other materials are dielectrics known in the art that are structurally sound so as to withstand processing conditions and field operating conditions. The dielectrics include, but are not ~~limited to~~ limited to, oxides, nitrides, carbides, carbon nitrides, oxynitrides, doped or slightly doped monocrystalline or polycrystalline silicon, and equivalents.

Please amend paragraph number [031] as follows:

[031] Because aluminum has a melting point of about ~~660°C~~, 660°C, substantially lower than that of tungsten (~~3,370°C~~) (3,370°C) or titanium (~~1,800°C~~), (1,800°C), achieving ductility sufficient to cause pressure or reflow filling of the contact hole comes at significantly lower temperatures for aluminum. For example, aluminum alone has a melting point that is about 26 percent of the melting point of tungsten, about 37 percent of the melting point of copper, and about 46 percent of the melting point of silicon. Adding preferred amounts of ~~copper~~ copper- and/or ~~silicon~~ silicon-~~alloying~~ alloying elements does not significantly cause the pressure fill or reflow temperatures to materially approach those required of a titanium plug fill in the contact hole (about 57 percent of tungsten) or of tungsten plug fill in the contact hole.

Please amend paragraph number [032] as follows:

[032] Figure 1 illustrates the first step in the inventive method in which a semiconductor device 10 has an insulation layer 14 disposed upon a semi-conductive device ~~underlying layer~~ substrate 12. A contact hole 16 has been formed, such as by patterning and etching, within insulation layer 14. Contact hole 16 exposes semiconductor substrate 12 and a first metallization layer 18 has been formed, such as by deposition, upon insulation layer 14.

Please amend paragraph number [033] as follows:

[033] Formation of first metallization layer 18 can be accomplished by physical vapor deposition (PVD), CVD, electroplating, and electroless plating. If first metallization layer 18 does not fill contact hole 16 when metallization layer 18 is formed, procedures for ~~filing~~ filling contact hole 16 are implemented. Various procedures are known to the art, such as pressure filling, reflow, and wetting layer-assisted reflow for CVD and PVD. For electroplating and electroless plating, the surface tension of the plating solution tended to resist the filling of a contact hole, particularly as the aspect ratio of the contact hole increases. As such, surfactants and/or other means of overcoming both surface tension and electrostatic charges must be employed to ensure that the contact hole is substantially completely filled.

Please amend paragraph number [034] as follows:

[034] Figure 2 illustrates the result of a pressure filling step in filling contact hole 16 with first metallization layer 18. A topographical depression forms in first metallization layer 18 above contact hole 16, caused by the filling of first metallization layer 18 into contact hole 16. Removal of at least some of first metallization layer 18 is next required to planarize the same. After formation of first metallization layer 18, an optional heat treatment is carried out to anneal ~~structure~~ structures of semiconductor device 10.

Please amend paragraph number [035] as follows:

[035] Figure 3 illustrates the result of a planarization step that stops on insulation layer 14. The planarizing step can be either a mechanical planarizing step or a chemical mechanical planarization step (CMP). After the planarization step, only a contact plug 19 remains of first metallization layer 18. Contact plug 19, which is isolated by ~~insulating~~ insulation layer 14, fills contact hole 16. A mechanical planarization step is costly in both time and materials. Mechanical planarization also requires a cleaning step before the wafer can be advanced to the next process step. If a chemical mechanical planarization process (CMP) is used to planarize and then stop on insulation layer 14, as shown in Figure 3, chemicals in the CMP process oxidize upper surfaces of first metallization layer 18 and abrasives therein shear away oxides of the upper surfaces of first metallization layer 18 in a repeating cycle that eventually planarizes first metallization layer 18.

Please amend paragraph number [036] as follows:

[036] Following planarization, a second metallization layer 20 seen in Figure 4 is formed upon insulation layer 14. Second metallization layer 20, like first metallization layer 18, can be formed by PVD, CVD, or variations thereof. Second metallization layer 20 is formed upon an exposed end of isolated contact plug 19. A second planarization step is carried out to planarize the exposed upper surface of second metallization layer 20. This second planarization step is performed until second metallization layer 20 has ~~of a~~ a preferred metallization line thickness. Like the first planarization step, the second ~~planarization~~ planarization step can be either a mechanical planarization step or a chemical mechanical planarization step.

Please amend paragraph number [037] as follows:

[037] By performing a second planarization step upon second metallization layer 20, the quality of planarity is achieved in which photolithographic restrictions upon depth-of-focus are ameliorated. Because of a planarity achieved by planarization that cannot be achieved merely by deposition, photographic notching is ~~minimized~~ minimized, as well as an irregular topography, both of which require a greater depth-of-focus.

Please amend paragraph number [039] as follows:

[039] Another method of the present invention, illustrated in Figure 6, involves forming sole metallization layer 22 upon insulation layer 14. If sole metallization layer 22 does not fill contact hole 16 when it is formed, procedures for ~~filling~~ filling contact hole 16 are implemented as described above. Planarization of sole metallization layer 22, such as by a mechanical or chemical-mechanical planarization process, is then undertaken. Planarization of sole metallization layer 22, however, does not expose insulation layer 14, but rather achieves a desired thickness upon insulation layer 14. Planarized sole metallization layer 22 and contact plug 19 are an integral structure, thus providing for one less metal-to-metal interface when compared with the structure ~~see~~ seen in Figures 4 and 5. Few metal-to-metal interfaces will correspondingly reduce resistance to current flow, in that a metal-to-metal interface may have discontinuities that cause resistance at the interface to be higher, which in turn causes the inherent inefficiency of Joule heating to occur.

Please amend paragraph number [041] as follows:

[041] The ~~forgoing~~ foregoing diffusion method can have the alternative of causing the diffusion from isolated contact plug 19 into second metallization layer 20. For example, where first metallization layer 18 has sufficient ductility qualities to substantially fill contact hole 16, but responds poorly to planarization, diffusion of a preferred alloying element from isolated contact plug 19 into second metallization layer 20 will create a substantially uniform concentration gradient profile of a preferred alloying element, but will not have affected the second planarization process of second metallization layer 20.

Please amend paragraph number [045] as follows:

[045] Another quality achieved in methods of the present invention is the avoidance of creating large and irregular grain structures in the metallization. These problematic grain structures are avoided when lower processing temperatures, such as those required for aluminum or a ~~lightly doped~~ lightly doped aluminum alloy, are used to fill contact hole 16. Because

aluminum has a melting point of about ~~660°C~~, 660°C, substantially lower than that of tungsten (~~3,370°C~~) (3,370°C) or titanium (~~1,800°C~~) (1,800°C), achieving ductility sufficient to cause pressure or reflow contact hole filling comes at significantly lower temperatures. For example, aluminum alone has a melting point that is about 26 percent that of tungsten, copper, about 37 percent, and silicon, about 46 percent. Adding preferred amounts of copper and/or silicon alloying elements does not significantly cause the pressure fill or reflow temperatures to materially approach those required of a titanium plug fill (about 57 percent of tungsten) or of a tungsten plug fill.

Please amend paragraph number [046] as follows:

[046] By maintaining lower temperatures, metal lines do not have the opportunity to form large or irregular grain structures. Such structures inhibit both metal reflow and planarization and ~~are therefore~~ are, therefore, to be avoided.

Please amend paragraph number [047] as follows:

[047] Another method of the present invention is illustrated in Figure 6. This method involves etching first metallization layer 18 to expose insulation layer 14, and then exposing lateral surfaces 24 of isolated contact plug 19. This method can be carried out by a single planarizing step, such as mechanical or chemical mechanical planarization, that will remove insulation layer 14 faster than first metallization layer 18 is removed, with some of each being removed by the planarizing step. When a chemical mechanical planarization step is used, the chemistry thereof requires that physically shearable surfaces are created in both first metallization layer 18 and in insulation layer 14, but that between these ~~two~~ two, the etch is more selective to first metallization layer 18 than insulation layer 14. An alternative to achieve the same structure with exposed lateral surfaces 24 is to stop on insulation layer 14 in a CMP step and conduct a second etch that is selective to isolated contact plug 19.

Please amend paragraph number [049] as follows:

[049] The present invention also includes a contact plug and metallization line structure according to Figures 7 and 8. The contact plug and metallization line structure includes semiconductor substrate 12 having a contact surface thereon. It also includes insulation layer 14 having contact hole 16 therethrough extending to the contact surface of semiconductor substrate 12. Additionally, it includes contact plug 19 substantially composed of a first metal and situated in contact hole 16, contact plug 19 being electrically insulated by insulation layer 14. Second metallization-~~line~~ layer 20 is substantially composed of a second metal, wherein contact plug 19 and second metallization-~~line~~ layer 20 are electrically connected and have a substantially continuous composition gradient of a selected alloying element between the first metal and ~~said~~ the second metal. The contact surface of semiconductor substrate 12 has first refractory metal silicide layer 30 thereon in contact with a first end of the plug 19. Contact hole 16 has an inside wall upon which a refractory metal nitride layer is situated in contact with the insulation layer and the plug. Additionally, contact plug 19 has a second end opposite the first end and in contact with a second refractory metal silicide layer 34 as seen in Figure 8. Second refractory metal silicide layer 34 is in contact with second metallization-~~line~~ layer 20.

Please amend paragraph number [050] as follows:

[050] The present invention also includes a contact plug and metallization line structure. The contact plug and metallization line structure includes semiconductor substrate 12 having situated thereon a silicon layer with a contact surface thereon. It also includes insulation layer 14 of BPSG on the silicon layer. Additionally, it includes contact hole 16 extending through insulation layer 14 of BPSG to the contact surface on the silicon layer. In addition thereto, it includes a refractory metal silicide layer 30 of titanium silicide on the contact surface of the silicon layer. Additionally, it includes refractory metal nitride lining 26 of titanium nitride on a sidewall of contact hole 16. Contact plug 19 is substantially composed of a first metal selected from the group consisting of Al, AlCu, and AlSiCu, and being situated in contact hole 16. Contact plug 19 is in contact, at an end thereof, with refractory metal silicide layer 30 of titanium silicide. Contact plug 19 has a sidewall in contact with refractory metal nitride lining 26 of

titanium nitride, and contact plug 19 is electrically insulated by insulation layer 14 of BPSG. Second metallization~~line~~ layer 20 is substantially composed of a second metal selected from the group consisting of Al, AlCu, and AlSiCu. One of the first and second metals has a higher concentration of Cu than the other of the first and second metals. Contact plug 19 and second metallization~~line~~ layer 20 are electrically connected and have a substantially continuous composition gradient of a selected alloying element between the first metal and the second metal, second metallization~~line~~ layer 20 having a substantially planar top surface. Contact plug 19 has first and second opposite ends each of which is in contact with refractory metal silicide materials 30, 34, respectively.

Please amend paragraph number [051] as follows:

[051] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes~~which~~ that come within the meaning and range of equivalency of the claims are to be embraced within their scope.